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IN THE CLAIMS:

Please replace the following claims for the same-numbered claims in the application:

1. (Currently Amended) A system level device for battery and integrated circuit chip integration comprising:

at least one solid state battery comprising battery cell arrays and control circuitry;

at least one integrated circuit chip powered by said at least one solid state battery; and

a package having a pair of opposed upright ends, said package connected to any of said at least one solid state battery and said at least one integrated circuit chip,

wherein said pair of opposed upright ends comprise a first end having a first upper surface and a second end having a second upper surface, wherein the first and second surfaces are substantially planar to one another,

wherein said at least one integrated circuit chip lays on top of a portion of said package, and

wherein said at least one solid state battery overhangs said at least one integrated circuit chip.

2. (Original) The device of claim 1, wherein said package connects to said at least one integrated circuit chip through an interior portion of said package.

3. (Previously Presented) The device of claim 1, wherein said at least one integrated circuit chip connects to an upper indent portion of said package, wherein said at least one solid state battery is larger than said at least one integrated circuit chip.

4. (Previously Presented) The device of claim 1, wherein said at least one solid state battery connects to an underside of said package.

5. (Currently Amended) A system level device for battery and integrated circuit chip integration comprising:

at least one solid state battery comprising battery cell arrays and control circuitry;

at least one integrated circuit chip powered by said at least one solid state battery; and

a package connected to any of said at least one solid state battery and said at least one integrated circuit chip,

wherein said at least one solid state battery connects to a pair of opposed upright ends of said package,

wherein said pair of opposed upright ends comprise a first end having a first upper surface and a second end having a second upper surface, wherein the first and second surfaces are substantially planar to one another.

wherein said at least one integrated circuit chip is disposed between said at least one solid state battery and said package, and

wherein said at least one integrated circuit chip lays on top of a portion of said package.

6. (Previously Presented) The device of claim 3, wherein said at least one solid state battery further comprises a stack of connected solid state batteries.

7. (Currently Amended) A system level device for battery and integrated circuit chip

integration comprising a multi-chip module integration system, wherein said multi-chip module integration system comprises:

a multi-chip module having a pair of opposed upright ends;

at least one solid state battery comprising battery cell arrays and control circuitry, said at least one solid state battery connected to said multi-chip module; and

at least one integrated circuit chip connected to said at least one solid state battery, wherein said integrated circuit chip is powered by said at least one solid state battery, and wherein said at least one solid state battery overhangs, and is larger than, said at least one integrated circuit chip,

wherein said pair of opposed upright ends comprise a first end having a first upper surface and a second end having a second upper surface, wherein the first and second surfaces are substantially planar to one another,

wherein said at least one integrated circuit chip lays on top of a portion of said multi-chip module.

8. (Currently Amended) The ~~device~~ system of claim 7, wherein said multi-chip module connects to said at least one integrated circuit chip through an interior portion of said multi-chip module.

9. (Currently Amended) The ~~device~~ system of claim 7, wherein said at least one integrated circuit chip connects to an upper indent portion of said multi-chip module.

10. (Currently Amended) A system level device for battery and integrated circuit chip

integration comprising a multi-chip module integration system, wherein said multi-chip module integration system comprises:

a multi-chip module;

at least one solid state battery comprising battery cell arrays and control circuitry, said at least one solid state battery connected to said multi-chip module; and

at least one integrated circuit chip connected to said at least one solid state battery, wherein said integrated circuit chip is powered by said at least one solid state battery,

wherein said at least one solid state battery connects to a pair of opposed upright ends of said multi-chip module,

wherein said pair of opposed upright ends comprise a first end having a first upper surface and a second end having a second upper surface, wherein the first and second surfaces are substantially planar to one another,

wherein said at least one solid state battery overhangs, and is larger than, said at least one integrated circuit chip, and

wherein said at least one integrated circuit chip lays on top of a portion of said multi-chip module.

11. (Currently Amended) An integrated chip structure comprising:

an integrated circuit chip;

a solid state battery comprising battery cell arrays and control circuitry, said at least one solid state battery directly connected to said integrated circuit chip; and

a package having a pair of opposed upright ends, said package connected to any of said solid state battery and said integrated circuit chip,

wherein an upper surface of said pair of opposed upright ends is planar with an upper surface of said integrated circuit chip,

wherein said integrated circuit chip lays on top of a portion of said package, and

wherein said solid state battery overhangs said at least one integrated circuit chip.

12. (Previously Presented) The structure in claim 11, further comprising solder connections between said solid state battery and said integrated circuit chip.

13. (Previously Presented) The structure in claim 12, wherein said solder connections comprise an electrical connection between said solid state battery and said integrated circuit chip.

14. (Previously Presented) The structure in claim 11, wherein said package surrounds said solid state battery and said integrated circuit chip.

15. (Previously Presented) The structure in claim 12, wherein said solid state battery is directly connected to said package.

16. (Currently Amended) An integrated chip structure comprising:

a package having a pair of opposed upright ends;

an integrated circuit chip mounted on said package;

a solid state battery comprising battery cell arrays and control circuitry, said at least one solid state battery directly connected to said package and electrically connected to said integrated circuit chip,

wherein said pair of opposed upright ends comprise a first end having a first upper surface and a second end having a second upper surface, wherein the first and second surfaces are substantially planar to one another,

wherein said integrated circuit chip lays on top of a portion of said package, and

wherein said solid state battery overhangs said at least one integrated circuit chip.

17. (Previously Presented) The structure in claim 16, wherein said solid state battery is held adjacent to said integrated circuit chip by said package.

18. (Previously Presented) The structure in claim 16, wherein said package is between said solid state battery and said integrated circuit chip.

19. (Previously Presented) The structure in claim 16, wherein said solid state battery is electrically connected to said integrated circuit chip through said package.

20. (Previously Presented) The structure in claim 16, wherein said solid state battery comprises multiple solid state batteries stacked on said package.